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(54) Title: A SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING A SEMICONDUCTOR DEVICE

(57) Abstract: A method is proposed for the fabrication of the gate electrode of a semiconductor device such that the effects of gate depletion are minimized. The method is comprised of a dual deposition process wherein the first step is a very thin layer that is doped very heavily by ion implantation. The second deposition, with an associated ion implant for doping, completes the gate electrode. With the two-deposition process, it is possible to maximize the doping at the gate electrode/gate dielectric interface while minimizing risk of boron penetration of the gate dielectric. A further development of this method includes the patterning of both gate electrode layers with the advantage of utilizing the drain extension and source/drain implants as the gate doping implants and the option of offsetting the two patterns to create an asymmetric device. A method is also provided for the formation of shallow junctions in a semiconductor substrate by diffusion of dopant from an implanted layer contained within a dielectric layer into the semiconductor surface. Further, the ion implanted layer is provided with a second implanted species, such as hydrogen, in addition to the intended dopant species, wherein said species enhances the diffusivity of the dopant in the dielectric layer.





INTERNATIONAL SEARCH REPORT

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B. FIEL	DS SEARCHED				
	ocumentation searched (classification system follower	d by classification symbols)			
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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)					
NONE					
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C. DOC	UMENTS CONSIDERED TO BE RELEVANT				
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International application No. PCT/US05/19085

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